This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Original) A photodetector for processing low luminous intensities comprising a monolithically integrated transimpedance amplifier and evaluation electronics, further comprising

an actual photocell portion (20) is associated with one chip side (R), from which preferably light (L) is incident,

an electronic circuit portion (30) is formed on the opposite chip side (V);

electric connections (40, 41) between said photocell portion (20) and the electronic circuit portion (30), said electric connections extending in a direction parallel to an orthogonal direction (chip normal) with respect to the chip plane.

2. (Original) The photodetector of claim 1, wherein said electric connections between said photocell portion (20) and said electronic circuit portion (30) are formed by (specifically) filled trenches (40, 41) doped in specified areas that are in particular extending in a crystalline semiconductor.

3. (Currently Amended) The photodetector of claims 1 or[[and]] 2, wherein said filled trenches comprise (conductively) doped sidewalls (41a, 41b), which form the at least one electric connection between said photocell portion (20) and said electronic circuit portion (30), and which particularly entirely extend through the crystalline semiconductor.

4. (Currently Amended) The photodetector of claims 1 or[[and]] 2, wherein filled trenches (40, 41) are filled with doped polysilicon for establishing said electric connections between said photocell portion (20) and said electronic circuit.

5. (Currently Amended) The photodetector of claim 2 ~~any claims 1 to 4~~, wherein said filled trenches are also used for an electrically non-conductive isolation (insulation) of different chip areas.

6. (Currently Amended) The photodetector of claim 2~~any claims 1 to 5~~, said photodetector being formed by CMOS or BiCMOS processes.

7. (Original) A method for forming a photodetector according to claim 1 for processing low luminous intensities, said photodetector comprising a monolithically integrated transimpedance amplifier and evaluation electronics (30), the method substantially comprising the steps of:

- using high-ohmic silicon (100 to 1000 Ohm * cm) of a first conductivity type, in particular a p-type, in a wafer as an initial material,
- forming an area of opposite conductivity type by counter-doping based on a mask, in particular by ion implantation, and subsequently annealing the wafer side (V) receiving the evaluation electronics (30);
- performing an epitaxy process for forming a layer having a thickness of substantially 10 to 25 µm and the first conductivity type of the initial material having a doping corresponding to a range of 5 to 50 Ohm * cm on the one wafer side;
- contacting the counter-doped layer now being buried (according to the second step) by locally providing a doping of the epitaxy layer by means of one of a Sinker diffusion and (specifically) filled trenches comprising doped areas;
- planarizing at least said filled trenches of the surface of the wafer side including said epitay layer;
- performing one of a (standard) CMOS and BiCMOS process for forming the integrated electronic circuit (30) on the one wafer side;
- thinning the wafer at the other side,
- in particular forming an antireflective coating above said one side;
- separating and mounting the chips and sealing the chips with a sealing material (61) that is optically transparent in a sensitive range of said photodetector.

8. (Original) The method of claim 7, for forming a photodetector, wherein

- after separating, said chips are mounted, with said one side (detector side), on a COL (chip on lead) carrier stripe, and said chips are electrically connected by bond wires in a conventional manner.

9. (Original) The method of claim 7 for forming a photodetector, wherein

after separating, the at least one chip is mounted with the side of the electronic circuit on a printed board or a lead frame (chip carrier stripe);

the mounted chip (10) is sealed with a sealing material (61) that is optically transparent in a sensitivity range of said photodetector.

10. (Currently Amended) A photodetector for processing low luminous intensities comprising monolithically integrated transimpedance amplifiers and evaluation electronics, i.e., photocell portion and evaluation electronics (20, 30) are formed in a common single crystalline semiconductor material,

the buried photocell portion and the overlying electronic circuit portions being associated with the chip front side (V);

electric connections being provided as trenches (40, 41) between said photocell portion and the electronic circuit portion, said electric connections extending in a direction of the chip normal or parallel with respect thereto;

for allowing light to be detected to be received from the backside (R) ~~(cf, Figure 1)~~.

11. (Currently Amended) The monolithic photodetector of claim 10, wherein said chip back side is configured for receiving said light to be detected ~~(cf., Figure 1)~~.

12. (Original) The monolithic photodetector of claim 10, wherein said electric connections (20) between said photocell portion and said electronic circuit are formed by specifically filled trenches doped in specified areas that are entirely extending within said crystalline semiconductor material.

13. (Currently Amended) The monolithic photodetector of claim 10 ~~any of claims 10 to 12~~, wherein said filled trenches (40) entirely extending within said single crystalline semiconductor material comprise sidewalls (41a, 41b) that are doped along the entire length so as to be conductive along the entire length, which form the electric connection betweens said photocell and said electronic circuit.

14. (Currently Amended) The monolithic photodetector of claim 10 ~~any of claims 10 to 12~~, wherein said specifically filled trenches (41) are filled with doped polysilicon for establishing said electric connections between said photocell and said electronic circuit.

15. (Currently Amended) The monolithic photodetector of claim 10 ~~any of claims 10 to 14~~, wherein said filled trenches provide for an electrically non-conductive isolation (insulation) of different chip areas.

16. (Currently Amended) The monolithic photodetector of claim 10 ~~any of claims 10 to 15~~, wherein said photodetector is formed by CMOS or BiCMOS processes.

17. (Original) A method for forming a photodetector for processing low luminous intensities according to claim 1, said photodetector comprising a monolithically integrated transimpedance amplifier and evaluation electronics, the method being characterized by the following manufacturing steps of:

17.1) using high-ohmic silicon (100 to 1000 Ohm*cm) of a first conductivity type,

17.2) forming an area of opposite conductivity type by counter-doping based on a mask, preferably by ion implantation, and subsequently

annealing the wafer front side (carrying the evaluation electronics in a later stage),

17.3) performing an epitaxy process for forming a layer having a thickness of 10 to 25 µm and the first conductivity type of the initial material having a doping corresponding to a range of 5 to 50 Ohm * cm at the wafer front side,

17.A1) contacting the counter-doped mask defined layer now being buried (according to the step 7.2) by specifically filled trenches,

17.A2) planarizing said filled trenches of the wafer front side,

17.4) performing one of a standard CMOS and BiCMOS process for forming the integrated electronic circuit on the wafer front side,

17.5) thinning the semiconductor wafer from the wafer backside,

17.6) after separating the chips, mounting the chips on the printed board or a lead frame (chip carrier stripe), said front side (the side carrying said electronic circuit) facing downwardly, and sealing said chip with a sealing material that is optically transparent in the sensitivity range of said photodetector.

18. (Original) The method of claim 17, wherein an order is determined by the continuous numbering.

19. (Original) The method of claim 17, wherein the steps 17.A1 and the subsequent step 17.A2 are always performed after step 17.3 or alternatively after step 17.4 or within the methodology of step 17.4.